WHAT IS CLAIMED IS:

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1. A processor comprising:

a segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication and a second operating mode indication;

a control register configured to store an enable indication, wherein said processor is configured to establish an operating mode responsive to said enable indication, said first operating mode indication, and said second operating mode indication.

2. The processor as recited in claim 1 wherein said operating mode is a first operating mode if said enable indication is in an enabled state and said first operating mode indication is in a first state, and wherein said operating mode is a second operating mode if said enable indication is in said enabled state, said first operating mode indication is in a second state, and said second operating mode indication is in said first state.

3. The processor as recited in claim 2 wherein said second operating mode is one of a plurality of operating modes available if said enable indication is in said enabled state and said first operating mode indication is in said second state, and wherein said one of said plurality of operating modes is selected in response to a state of said second operating mode indication.

4. The processor as recited in claim 3 wherein one of said plurality of operating modes is a 32 bit operating mode.

5. The processor as recited in claim 3 wherein one of said plurality of operating modes is

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a 16 bit operating mode.

6. The processor as recited in claim 2 wherein said first operating mode includes a default address size which is greater than 32 bits.

7. The processor as recited in claim 6 wherein said default address size applies to virtual addresses generated by said processor.

8. The processor as recited in claim 7 wherein a virtual address is generated according to a segmentation mechanism employed by said processor.

9. The processor as recited in claim 7 wherein said default address size further applies to physical addresses generated by said processor.

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10. ~~The~~ processor as recited in claim 1 wherein, if said enable indication is in a disabled state, said first operating mode indication ~~is undefined and~~ said processor is configured to establish said operating mode responsive to said second operating mode indication~~.~~

11. A processor comprising:

a segment register configured to store a segment selector and information from a segment descriptor, wherein said segment selector includes an index into a segment descriptor table stored in a memory to which said processor is coupled, said segment descriptor stored in said segment descriptor table in an entry indicated by said index, wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said segment selector, said segment descriptor including an operating mode indication; and

a control register configured to store an enable indication;

wherein said processor is configured to operate in an operating mode in which virtual addresses are greater than 32 bits responsive to said enable indication being in an enabled state and said operating mode indication being in a first state.

12. The processor as recited in claim 11 wherein physical addresses are greater than 32 bit in said operating mode.

13. The processor as recited in claim 12 wherein physical addresses are a first number of bits less than or equal to 64 bits.

14. The processor as recited in claim 11 wherein virtual addresses are a first number of bits less than or equal to 64 bits.

15. The processor as recited in claim 11 wherein said segment descriptor further includes a privilege level.

16. The processor as recited in claim 11 further comprising a second control register configured to store a second enable indication, wherein said processor is configured to read said segment descriptor from said segment descriptor table responsive to said second enable indication being in said enabled state.

17. A method comprising:

establishing an operating mode in a processor in response to an enable indication in a control register within said processor, a first operating mode indication in a segment descriptor, and a second operating mode indication in said segment descriptor;

fetching operands and generating addresses in response to said operating mode.

18. The method as recited in claim 17 wherein said establishing comprises establishing a first operating mode responsive to said enable indication being in an enabled state and said first operating mode indication being in a first state, and wherein said first operating mode includes a default address size greater than 32 bits.

19. The method as recited in claim 18 wherein said default address size applies to a virtual address.

20. The method as recited in claim 19 wherein said default address size applies to a physical address.

21. The method as recited in claim 18 wherein said establishing further comprises establishing a second operating mode responsive to said enable indication being in an enabled state, said first operating mode indication being in a second state, and said second operating mode being in said first state, and wherein said first operating mode includes a default address size of 32 bits.

22. The method as recited in claim 18 wherein said establishing further comprises establishing one of a plurality of operating modes if said enable indication is in said enabled state and said first operating mode indication is in a second state, and wherein said one of said plurality of operating modes is selected in response to a state of said second operating mode indication.